UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,937	09/29/2003	Fred Gehrung Gustavson	YOR920030171US1	8297

48150   7590   10/16/2007

MCGINN INTELLECTUAL PROPERTY LAW GROUP, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER
WEI, ZHENG

ART UNIT	PAPER NUMBER
2192	

MAIL DATE	DELIVERY MODE
10/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _27 July 2007_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-20_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-20_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _30 December 2003_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _See Continuation Sheet_.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____ .

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :08/08/07, 07/31/07, 06/19/07, 05/03/07, 03/30/07.

DETAILED ACTION

Remarks

1.   This office action is in response to the amendment filed on 07/27/2007.

2.   Claims 1, 2, 4, 6, 8, 10 and 12-19 have been amended.

3.   Claim 20 has been added

4.   The 35 U.S.C. 101 rejections of claims 1-19 are withdrawn in view of the

Applicant's amendment.

5.   Claims 1-20 remain pending and have been examined.

Information Disclosure Statement

6.   The information disclosure statements filed on 08/08/2007 has been placed in

the application file and the information referred to therein has already been

considered.

Drawings

7.   The drawings filed on September 29, 2003 and the replacement drawing filed on

December 30, 2003 are not accepted by the Examiner because of on-compliance

with 37 CFR § 1.12(d). Any changes to an application drawing must be in

compliance with 37 CFR § 1.84 and must be submitted on a replacement sheet

of drawings, which shall be an attachment to the amendment document and, in

the top margin, labeled "Replacement Sheet".

The replacement sheet of FIG. 1-5 **should be labeled "Replacement Sheet" in**

the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the

drawing figures. If the changes are not accepted by the Examiner, the Applicant

will be notified and informed of any required corrective action in the next Office

Action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

8.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9.   Claims 4, 5, 9, 10, 15, 16 and 18-20 rejected under 35 U.S.C. 112, second

paragraph, as being indefinite for failing to particularly point out and distinctly

claim the subject matter which applicant regards as the invention.

Claims 4, 9, 15 and 18:

These claims direct to a subroutine which is equivalent to a LAPACK subroutine.

However, the limitations, such as "as modified in accordance with claim 1", lack

of antecedent basis and thus are indefinite.

Claims 5, 10, 16 and 19:

These claims are dependent claims of claims 4, 9, 15 and 18. Therefore are also

rejected for the same reason.

Claim 20:

The term "n cycles" in claim 20 is a relative term which renders the claim

indefinite. The term "n cycles" is not defined by the claim, the specification does

not provide a standard for ascertaining the requisite degree, and one of ordinary

skill in the art would not be reasonably apprised of the scope of the invention.

For the purpose of compact prosecution, the examiner treats "n cycles" as –one

or more cycles--.

Claim Rejections - 35 USC § 103

10.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set
forth in section 102 of this title, if the differences between the subject matter sought to be patented and
the prior art are such that the subject matter as a whole would have been obvious at the time the
invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negatived by the manner in which the invention was made.

11.   Claims 1, 2 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by

Nakazawa (Nakazawa et al., US 5,438,669) in view of Dhablania (US 6,115,730)

Claim 1:

Nakazawa discloses a software method of executing a linear algebra subroutine,

said method comprising: for an execution code controlling operation of a floating

point unit (FPU) performing said linear algebra subroutine execution, using

preload instruction to preload data into a floating point register (FRegs) of said

FPU. (see for example, Fig.3, element 105, "Physical Floating Point Register

Group", element 106 "Floating Point Calculator", element 102 "Instruction

Controller" and related; Also see, Fig.4B, 4C "Floating Point Register Preload

Instruction", "Extended Floating Point Register Preload Instruction" and related

text"; Further see, col.7, lines 2-11, "the program by the loop unrolling method

requires four floating point registers and one general register for vector data

storage...")

But Nakazawa does not explicitly disclose the detailed method about overlapping

by preloading data. However, Dhablania in the same analogous art of reloadable

floating point unit, discloses a software method of improving at least one of

efficiency and speed in executing a linear algebra subroutine on a computer

having a floating point unit (FPU) and a load/store unit (LSU) capable of

overlapping loading data and processing of said data by the FPU, said method

comprising:

- For an execution code controlling operation of said linear algebra subroutine

  execution, overlapping by preloading data into a floating point registers

  (Fregs) of said FPU, said overlapping causing data to arrive into said Fregs to

  be timely executed by the FPU operations of said linear algebra subroutine on

  said FPU (see for example, Fig.4a, 4b and related text; also see col.1, section

  "Summary of the invention", "ability to initiate a next instruction held in a 4-

  deep instruction queue before a prior instruction has finished"; col.4, lines 21-

26, "The FPU 70 includes a load/store stage with 4-deep load and store

queues")

Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to use the method disclosed by <u>Nakazawa</u> and

<u>Dhablania</u> to improve the performance of an FPU by providing it with preload

registers which enable initiation of a next instruction held in a instruction queue

as suggested by <u>Dhablania</u> (see for example, col.1, Summary of the invention)

Claim 2:

<u>Nakazawa</u> and <u>Dhablania</u> disclose the method of claim 1, <u>Nakazawa</u> further

discloses wherein said instructions are unrolled repeatedly until the data loading

reaches a steady state in which a data loading exceeds a data consumption (see

for example, col.5, lines 23-28, "With this loop unrolling method, a plurality of

elements (=n) are processed in one loop, this loop unrolling method has 1/n the

number of loops required by the conventional method", also see Fig.11 and 12

for unrolling results and related text).

Claim 20:

<u>Nakazawa</u> and <u>Dhablania</u> disclose the method of Claim 1, <u>Dhablania</u> further

discloses wherein said FPU comprises said Fregs as interfaced with an L1

cache, said interface having a penalty of n cycles, said preloading eliminating this

n-cycle penalty (see for example, Fig1a, element 60, 29 "Unified Cache", "Write

Buffer"; also see col.10, lines 58-67, "eliminate a full cycle form time period" and
related text)

Claim 17:

Nakazawa discloses a method of providing a service involving at least one of
solving and applying a scientific/engineering problem, said method comprising at
least one of: using a linear algebra software package that computes one or more
matrix subroutines, wherein said linear algebra software package generates an
execution code controlling a load/store unit loading data into a floating point
register (FReg) for a floating point unit (FPU) performing a linear algebra
subroutine execution, such that, for an execution code controlling operation of
said FPU, an instruction is unrolled to cause a preloading of data into said FReg.
(see for example, Fig.3, element 105, "Physical Floating Point Register Group",
element 106 "Floating Point Calculator", element 102 "Instruction Controller" and
related; Also see, Fig.4B, 4C "Floating Point Register Preload Instruction",
"Extended Floating Point Register Preload Instruction" and related text"; Further
see, col.7, lines 2-11, "the program by the loop unrolling method requires four
floating point registers and one general register for vector data storage...");
But Nakazawa does not explicitly disclose the detailed method about overlapping
by preloading data. However, Dhablania in the same analogous art of reloadable
floating point unit, discloses a software method of improving at least one of
efficiency and speed in executing a linear algebra subroutine on a computer

having a floating point unit (FPU) and a load/store unit (LSU) capable of

overlapping loading data and processing of said FPU data by the FPU, said

method comprising:

- For an execution code controlling operation of said linear algebra subroutine

  execution, overlapping by preloading data into a floating point registers

  (Fregs) of said FPU, said overlapping causing data to arrive into said Fregs to

  be timely executed by the FPU operations of said linear algebra subroutine on

  said FPU (see for example, Fig.4a,4b and related text; also see col.1, section

  "Summary of the invention", "ability to initiate a next instruction held in a 4-

  deep instruction queue before a prior instruction has finished"; col.4, lines 21-

  26, "The FPU 70 includes a load/store stage with 4-deep load and store

  queues")

Therefore, it would have been obvious to one having ordinary skill in the art at

the time the invention was made to use the method disclosed by Nakazawa and

Dhablania to improve the performance of an FPU by providing it with preload

registers which enable initiation of a next instruction held in a instruction queue

as suggested by Dhablania (see for example, col.1, Summary of the invention).

Dhablania also discloses providing a consultation for purpose of solving a

scientific/engineering problem using said linear algebra software package (see

for example, col.1, section "Summary of the invention");

But neither of them explicitly discloses transmitting a result of said linear algebra

software package on at least one of a network, a signal-bearing medium

containing machine-readable data representing said result, and a printed version representing said result; and receiving a result of said linear algebra software package on at least one of a network, a signal-bearing medium containing machine-readable data representing said result, and a printed version representing said result. However, it is well known in the computer the result (data) of said executing linear algebra software package can be transmitted, stored and printed. Thus, it also would have been obvious.

12.   Claims 3-16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakazawa (Nakazawa et al., US 5,438,669) in view of Dhablania (US 6,115,730) and further in view of Dongarra (Dongarra et al., "A Set of Level 3 Basic Linear Algebra Subprograms")

Claim 3:

Nakazawa and Dhablania disclose the method of claim 1, but neither of them explicitly discloses wherein said linear algebra subroutine comprises a matrix multiplication operation. However, Dongarra in the same analogous art of implementation of Level 3 Basic Linear Algebra Subprograms discloses matrix multiplication operation (matrix- multiply) (see for example, p.11, line 15, "matrix-multiply routine"). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use Nakazawa's calculator to do matrix multiplication operation. One would have been motivated to do so to improve efficiency and parallel processing capability as suggested by Dongarra

(see for example, p.1, abstract portion, lines 1-4, "The Level 3 BLAS are targeted at matrix-matrix operations, with the aim of providing more efficient, but portable, implementations of algorithms on high-performance computers, especially those with hierarchical memory and parallel processing capability.")

Claim 4:

Nakazawa and Dhablania disclose the method of claim 1, but does not explicitly disclose wherein said linear algebra subroutine comprises a subroutine equivalent to a LAPACK (Linear Algebra PACKage) subroutine, as modified in accordance with claim 1. However, Dongarra in the same analogous art of linear algebra discloses LAPACK (LINPACK) (see for example, p.1, Introduction, "The original basic linear algebra subprograms...have been used in a wide range of software including LINPACK [13]..."). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use existing routine defined or implemented by LINAPACK. One would have been motivated to do so to greatly simplify the implementation of the infrastructure as suggested by Dongarra (see for example, p.1-2, Introduction "In particular, they are an aid to clarity, portability, modularity, and maintenance of software; and they have become a de facto standard for the elementary vector operations.")

Claim 5

Nakazawa, Dhablania and Dongarra disclose the method of claim 4, Dongarra

further discloses said LINPACK subroutine comprises a BLAS Level 3 L1 cache

kernel (see for example, p.2, Introduction, "For example, no routines are included

for matrix factorization; these are currently provided by LINPACK and will be

included in a new linear algebra package currently under development...").

Claim 18:

Nakazawa and Dhablania disclose the method of claim 17, but neither of them

explicitly discloses wherein said linear algebra subroutine comprises a subroutine

from a LAPACK (Linear Algebra PACKage). However, Dongarra in the same

analogous art of linear algebra discloses LAPACK (LINPACK) (see for example,

p.1, Introduction, "The original basic linear algebra subprograms...have been

used in a wide range of software including LINPACK [13]..."). Therefore, it would

have been obvious to one having ordinary skill in the art at the time the invention

was made to use existing routine defined or implemented by LINAPACK. One

would have been motivated to do so to greatly simplify the implementation of the

infrastructure as suggested by Dongarra (see for example, p.1-2, Introduction "In

particular, they are an aid to clarity, portability, modularity, and maintenance of

software; and they have become a de facto standard for the elementary vector

operations.")

Claim 19:

Nakazawa, Dhablania and Dongarra disclose the method of claim 18, Dongarra further discloses said LINPACK subroutine comprises a BLAS Level 3 L1 cache kernel (see for example, p.2, Introduction, "For example, no routines are included for matrix factorization; these are currently provided by LINPACK and will be included in a new linear algebra package currently under development...").

Claims 6-11:

Claims 6-11 are an apparatus version of claimed method, wherein all claimed limitations have been address and/or set forth above in claims 1-5. Therefore, as the references teach all the limitation of claims 1-5, they also teach the limitations of claims 6-11 respectively. Thus, they also would have been obvious.

Claims 12-16:

Claims 12-16 are a software program product version of claimed method, wherein all claimed limitations have been address and/or set forth above in claims 1-5. Therefore, as the references teach all the limitation of claims 1-5, they also teach the limitations of claims 12-16 respectively. Thus, they also would have been obvious.

Conclusion

13.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in

37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed

within TWO MONTHS of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory

period, then the shortened statutory period will expire on the date the advisory

action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be

calculated from the mailing date of the advisory action. In no event, however, will

the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

14.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Zheng Wei whose telephone number is (571)

270-1059 and Fax number is (571) 270-2059. The examiner can normally be

reached on Monday-Thursday 8:00-15:00.

If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is 571- 272-1000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ZW

TUAN DAM
SUPERVISORY PATENT EXAMINER